

What is claimed is:

1. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

a ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port; and

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means, whereby in detecting a presence of said electrostatic pulse said ESD pulse detection means generates a voltage that triggers said ESD pulse clamp means thereby shunting said electrostatic pulse from said IC.

2. The circuit of claim 1 wherein said ESD pulse detection means contains a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter.
3. The circuit of claim 2 wherein said voltage inverter comprises a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port.
4. The circuit of claim 3 wherein said first port of said voltage inverter is connected to said first terminal of said IC, while said second port of said voltage inverter is connected to said second terminal of said IC.
5. The circuit of claim 3 wherein said connections of gate of said PMOS device and of said NMOS device are commonly connected to said third port of said voltage inverter.
6. The circuit of claim 3 wherein said connection of drain and said connection of bulk of said PMOS device are commonly connected to said first port of said voltage inverter.

7. The circuit of claim 3 wherein said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter.

8. The circuit of claim 3 wherein said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter.

9. The circuit of claim 2 wherein said capacitive component has a first terminal and a second terminal, said first terminal of said capacitive component is connected to said first terminal of said IC, said resistive component has a first terminal and a second terminal, said second terminal of said resistive component is connected to said second port of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component are commonly connected to said third port of said voltage inverter.

10. The circuit of claim 1 wherein said ESD pulse clamp means comprises a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port.

11. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said PMOS device is connected to said third port of said ESD pulse clamp means.

12. The circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises:

a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component; and

a NMOS device having connections of gate electrode, source, drain and bulk whereby said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is

connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component.

13. The circuit of claim 2 wherein said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

14. The circuit of claim 2, wherein:

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive, said capacitive component further comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component,

said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component; and

said resistive component comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connection of gate is connected via a resistive load to said second terminal of said resistive component, said connection of source is connected to said second terminal of said resistive component, said connections of drain and of bulk are commonly connected to said first terminal of said resistive load.

15. The circuit of claim 2 wherein:

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component; and

said resistive component of said ESD pulse detection means comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connections of source and bulk of

said NMOS device are commonly connected to said second terminal of said resistive component, said connection of gate is connected via a resistive load to said first terminal of said capacitive component, said connection of drain of said NMOS device is connected to said first terminal of said resistive component.

16. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

17. The circuit of claim 16 wherein said capacitive component of said ESD pulse detection means comprises parasitic capacitance

that is present between said third port of said voltage inverter and said first terminal of said IC.

18. The circuit of claim 10 wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device to connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS device, said connection of source said PMOS device is connected to said first port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said second port of said IC, said connection of gate of said PMOS device is connected to said first port of said ESD pulse clamp means via a resistive load.

19. The circuit of claim 18 wherein said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first terminal of said IC.

20. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component, a capacitive component, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage

A5

said capacitive component of said ESD pulse detection means

said resistive component of said ESD pulse detection means

As said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

21. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage

inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component, said capacitive component also comprising a NMOS device having connections of gate electrode, source, drain and bulk whereby said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

46

potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said

Handwritten: 2940950

NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk whereby said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component.

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second

port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

23. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said second terminal of said capacitive component, said connection of gate is connected to said first terminal of said capacitive component, said capacitive component further comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connection of gate electrode is connected via a resistive load component to said second terminal of said capacitive component, said connection of source is connected to said second terminal of said capacitive component, said connection of drain is connected to said first terminal of said capacitive component, said connection of bulk is connected to said second terminal of said resistive component;

51

component, said connections of drain and of bulk are commonly connected to said first terminal of said resistive load; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate of said PMOS device is connected to said third port of said ESD pulse clamp means.

24. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to

extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said

voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter; said capacitive component of said ESD pulse detection means comprises a PMOS device having connections of gate electrode, source, drain and bulk, said connections of source, drain and bulk of said PMOS device are commonly connected to said first terminal of said capacitive component, said connection of gate is connected to said second terminal of said capacitive component;

said resistive component of said ESD pulse detection means comprises a NMOS device having connections of gate electrode, source, drain and bulk, said connections of source and bulk of said NMOS device are commonly connected to said second port of said resistive component, said connection of gate is connected via a resistive load to said first port of said capacitive component, said connection of drain of said NMOS device is connected to said first terminal of said resistive component; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second

port and a third port, said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said ESD pulse clamp means, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of gate said PMOS device is connected to said third port of said ESD pulse clamp means.

25. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component of said pulse detector and said first terminal of said resistive component of said pulse detector being commonly connected to said third port of said voltage inverter; said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of

said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

26. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second

terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connection of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device is commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprising a first terminal and a second terminal, said first terminal of said capacitive component being connected to said first terminal of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said capacitive component and said first terminal of said resistive component being commonly connected to said third port of said voltage inverter; and

said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device to connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS device, said connection of source said PMOS device is connected to said first port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said second port of said IC, said connection of gate of said PMOS device is connected to said first port of said ESD pulse clamp means via a resistive load.

27. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has

as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is

connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first port of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second port of said IC, and said first terminal of said being connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, said first port of said ESD pulse clamp

means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of source of said PMOS device is connected to said second port of said ESD pulse clamp means, said connection of drain of said PMOS device is connected to said first port of said voltage inverter, said connection of gate of said PMOS device is connected to said third port of said voltage inverter, said connection of bulk of said PMOS device is connected to said connection of gate of said PMOS device via well resistance that is present in the N-well underlying said PMOS device.

28. An Electrostatic Discharge (ESD) protection circuit that is connected between a first terminal and a second terminal of an Integrated Circuit (IC), whereby said ESD protection circuit has as objective to dissipate an electrostatic pulse that originates from an ESD source that is connected between said first terminal and said second terminal thereby protecting said IC from potential damage that can be caused by exposure of said IC to extreme values of voltage from said ESD source, whereby said ESD protection circuit comprises:

an ESD pulse clamp means for shunting said electrostatic pulse from said IC having a first port that is connected to said

first terminal of said IC, a second port that is connected to said second terminal of said IC, and a third port;

an ESD pulse detection means having a first input port connected to said first terminal of said IC, a second input port connected to said second terminal of said IC, an output port that is connected to said third port of said ESD pulse clamp means;

said ESD pulse detection means containing a network comprising a resistive component having a first and a second terminal, a capacitive component having a first and a second terminal, and a voltage inverter;

said voltage inverter of said ESD pulse detection means comprising a PMOS device having connections of gate electrode, source, drain and bulk, and a NMOS device having connections of gate electrode, source, drain and bulk, whereby said voltage inverter contains a first port, a second port, a third port, and a fourth port, said first port of said voltage inverter is connected to said first terminal of said IC, said second port of said voltage inverter is connected to said second terminal of said IC, said connections of gate of said PMOS device and said NMOS device are commonly connected to said third port of said voltage inverter, said connections of bulk and drain of said PMOS device are commonly connected to said first port of said voltage inverter, said connection of source and said connection of bulk of said NMOS device are commonly connected to said second port of

said voltage inverter, said connection of source of said PMOS device and said connection of drain of said NMOS device are commonly connected to said fourth port of said voltage inverter;

said capacitive component of said ESD pulse detection means comprises parasitic capacitance that is present between said third port of said voltage inverter and said first port of said IC;

said resistive component of said ESD pulse detection means comprising a first terminal and a second terminal, said second terminal of said resistive component being connected to said second terminal of said IC, and said second terminal of said resistive component being connected to said third port of said voltage inverter; and

said ESD pulse clamp means comprising a PMOS device having connections of gate electrode, source, drain and bulk, whereby said ESD pulse clamp means contains a first port and a second port and a third port, wherein said first port of said ESD pulse clamp means is connected to said first terminal of said IC, said second port of said ESD pulse clamp means is connected to said second terminal of said IC, said third port of said ESD pulse clamp means is connected to said fourth port of said voltage inverter, said connection of bulk of said PMOS device is connected to said third port of said ESD pulse clamp means via well resistance that is present in a N-well underlying said PMOS

1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 11
 12
 13
 14
 15
 16
 17
 18
 19
 20
 21
 22
 23
 24
 25
 26
 27
 28
 29
 30
 31
 32
 33
 34
 35
 36
 37
 38
 39
 40
 41
 42
 43
 44
 45
 46
 47
 48
 49
 50
 51
 52
 53
 54
 55
 56
 57
 58
 59
 60
 61
 62
 63
 64
 65
 66
 67
 68
 69
 70
 71
 72
 73
 74
 75
 76
 77
 78
 79
 80
 81
 82
 83
 84
 85
 86
 87
 88
 89
 90
 91
 92
 93
 94
 95
 96
 97
 98
 99
 100
 101
 102
 103
 104
 105
 106
 107
 108
 109
 110
 111
 112
 113
 114
 115
 116
 117
 118
 119
 120
 121
 122
 123
 124
 125
 126
 127
 128
 129
 130
 131
 132
 133
 134
 135
 136
 137
 138
 139
 140
 141
 142
 143
 144
 145
 146
 147
 148
 149
 150
 151
 152
 153
 154
 155
 156
 157
 158
 159
 160
 161
 162
 163
 164
 165
 166
 167
 168
 169
 170
 171
 172
 173
 174
 175
 176
 177
 178
 179
 180
 181
 182
 183
 184
 185
 186
 187
 188
 189
 190
 191
 192
 193
 194
 195
 196
 197
 198
 199
 200
 201
 202
 203
 204
 205
 206
 207
 208
 209
 210
 211
 212
 213
 214
 215
 216
 217
 218
 219
 220
 221
 222
 223
 224
 225
 226
 227
 228
 229
 230
 231
 232
 233
 234
 235
 236
 237
 238
 239
 240
 241
 242
 243
 244
 245
 246
 247
 248
 249
 250
 251
 252
 253
 254
 255
 256
 257
 258
 259
 260
 261
 262
 263
 264
 265
 266
 267
 268
 269
 270
 271
 272
 273
 274
 275
 276
 277
 278
 279
 280
 281
 282
 283
 284
 285
 286
 287
 288
 289
 290
 291
 292
 293
 294
 295
 296
 297
 298
 299
 300
 301
 302
 303
 304
 305
 306
 307
 308
 309
 310
 311
 312
 313
 314
 315
 316
 317
 318
 319
 320
 321
 322
 323
 324
 325
 326
 327
 328
 329
 330
 331
 332
 333
 334
 335
 336
 337
 338
 339
 340
 341
 342
 343
 344
 345
 346
 347
 348
 349
 350
 351
 352
 353
 354
 355
 356
 357
 358
 359
 360
 361
 362
 363
 364
 365
 366
 367
 368
 369
 370
 371
 372
 373
 374
 375
 376
 377
 378
 379
 380
 381
 382
 383
 384
 385
 386
 387
 388
 389
 390
 391
 392
 393
 394
 395
 396
 397
 398
 399
 400
 401
 402
 403
 404
 405
 406
 407
 408
 409
 410
 411
 412
 413
 414
 415
 416
 417
 418
 419
 420
 421
 422
 423
 424
 425
 426
 427
 428
 429
 430
 431
 432
 433
 434
 435
 436
 437
 438
 439
 440
 441
 442
 443
 444
 445
 446
 447
 448
 449
 450
 451
 452
 453
 454
 455
 456
 457
 458
 459
 460
 461
 462
 463
 464
 465
 466
 467
 468
 469
 470
 471
 472
 473
 474
 475
 476
 477
 478
 479
 480
 481
 482
 483
 484
 485
 486
 487
 488
 489
 490
 491
 492
 493
 494
 495
 496
 497
 498
 499
 500
 501
 502
 503
 504
 505
 506
 507
 508
 509
 510
 511
 512
 513
 514
 515
 516
 517
 518
 519
 520
 521
 522
 523
 524
 525